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AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. – 2. (Cancelled)
3. (Currently amended) A circuit package, comprising:
a dielectric substrate having a first surface and a ~~second surface~~ conductive layer,
~~disposed opposite to said first surface~~, and a via extending therebetween, with a
first conductor disposed on said first surface ~~and extending from said via~~, and a
~~second conductor disposed on said second surface and extending from said via~~,
with said via placing said first conductor and ~~second conductors~~ said conductive
layer in electrical communication;
a driver circuit mounted to said substrate and including an input and an output, with said
output being in electrical communication with said first conductor and having an
output resistive component associated therewith, with said via having a resistive
fill disposed therein, defining a via resistance connected between said first
conductor and ~~second conductors~~ and said conductive layer, said output having an
output impedance being defined by said output resistive component and said via
resistance; and
wherein said substrate further includes an additional conductor and an additional via
filled with said resistive fill, defining an additional via resistance, said additional
conductor being disposed on said first surface ~~and extending from said additional
via~~, with said ~~a second conductor~~ conductive layer being in electrical
communication with said additional via with said additional via resistance
extending between said additional conductor and ~~said second conductors~~
conductive layer and said input being in electrical communication with said
additional conductor and having an input resistance component and an input
impedance associated therewith, with said input impedance being defined by said
input resistive component and said additional via resistance.
4. (Currently amended) A circuit package, comprising:

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a dielectric substrate having a first surface and a ~~second surface~~ conductive layer,
~~disposed opposite to said first surface;~~ and a via extending therebetween, with a
first conductor disposed on said first surface ~~and extending from said via;~~ and a
~~second conductor disposed on said second surface and extending from said via,~~
with said via placing said first conductor and ~~second conductors~~ said conductive
layer in electrical communication;

a driver circuit mounted to said substrate and including an input and an output, with said
output being in electrical communication with said first conductor and having an
output resistive component associated therewith, with said via having a resistive
fill disposed therein, defining a via resistance connected between said first
conductor and ~~second conductors~~ said conductive layer, said output having an
output impedance being defined by said output resistive component and said via
resistance; and

wherein said substrate includes a plurality of said via, individual ones of a subgroup of
said via which in electrical communication and extending extends between said
first surface and ~~second conductors~~ said conductive layer in parallel and have said
resistive fill disposed therein to define said via resistance, with said via resistance
being inversely proportional to a number of said plurality of vias in said subgroup.

5. (Currently amended) A circuit package, comprising:

a dielectric substrate having a first surface and a ~~second surface~~ conductive layer,
~~disposed opposite to said first surface;~~ and a via extending therebetween, with a
first conductor disposed on said first surface ~~and extending from said via;~~ and a
~~second conductor disposed on said second surface and extending from said via,~~
with said via placing said first conductor and ~~second conductors~~ said conductive
layer in electrical communication;

a driver circuit mounted to said substrate and including an input and an output, with said
output being in electrical communication with said first conductor and having an
output resistive component associated therewith, with said via having a resistive
fill disposed therein, defining a via resistance connected between said first
conductor and ~~second conductors~~ and said conductive layer, said output having an

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output impedance being defined by said output resistive component and said via resistance; and

wherein said via resistance has a magnitude that is at least twice a magnitude of said output resistive component.

6. (Currently amended) A circuit package, comprising:
a dielectric substrate having a first surface and a ~~second surface~~ conductive layer,
~~disposed opposite to said first surface~~, and a via extending therebetween, with a first conductor disposed on said first surface ~~and extending from said via~~, and a ~~second conductor disposed on said second surface and extending from said via~~, with said via placing said first conductor and ~~second conductors~~ said conductive layer in electrical communication;
a driver circuit mounted to said substrate and including an input and an output, with said output being in electrical communication with said first conductor and having an output resistive component associated therewith, with said via having a resistive fill disposed therein, defining a via resistance connected between said first conductor and ~~second conductors~~ and said conductive layer, said output having an output impedance being defined by said output resistive component and said via resistance; and
wherein said output resistive component further includes an output resistance of said driver circuit having a magnitude in a range of 5 to 12 ohms, inclusive, with said via resistance having a magnitude in a range of 35 to 50 ohms, inclusive.

7. (Previously presented) The circuit package as recited in claim 5 wherein said substrate comprises a printed circuit board.

8. (Previously presented) The circuit package as recited in claim 5 wherein said driving circuit is selected from a set of driving circuits consisting of, a buffer, an inverter and an amplifier.

9. (Currently amended) A circuit, comprising:

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a dielectric substrate having a first surface and a ~~second surface~~ first conductive layer and a second conductive layer, ~~disposed opposite to said first surface~~ and a plurality of vias extending therebetween, with first and second conductors disposed on said first surface and ~~a third conductor disposed on said second surface~~, with said first and third conductors ~~and extending from a first of said plurality of vias and said second and third conductors extending from a second of said plurality of vias~~;

a driver circuit mounted to said substrate and including an output having an output resistive component associated therewith, and an input having an input resistive component associated therewith, with said output being in electrical communication with said first conductor and said input being in electrical communication with said second conductor, with ~~said a first via of said plurality of vias~~ of vias having a resistive fill disposed therein defining a first via resistance connected between said first conductor and ~~third conductors~~ and said first conductive layer and ~~said a second via of said plurality of vias~~ of said plurality of vias having said resistive fill disposed therein defining a second via resistance connected between said second conductor and ~~third conductors~~ said second conductive layer, with said output having an output impedance associated therewith defined by said output resistive component and said first via resistance, with said first via resistance, having a magnitude that is at least twice a magnitude of said output resistive component, with said input having an input impedance associated therewith defined by said input resistive component and said second via resistance, with said second via resistance having a magnitude that is at least twice a magnitude of said input resistive component.

10. (Currently amended) The circuit package as recited in claim 9 wherein a first subgroup of said plurality of said vias extends between said first surface and ~~third conductors~~ said first conductive layer in parallel and have said resistive fill disposed therein to define said first resistance, with said first resistance being inversely proportional to a number of said plurality of vias in said first subgroup.

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11. (Currently amended) The circuit package as recited in claim 10 wherein a second subgroup of said plurality of said vias extends between said ~~second~~ first surface and ~~third conductors~~ said second conductive layer in parallel and have said resistive fill disposed therein to define said second resistance, with said second resistance being inversely proportional to a number of said plurality of vias in said first subgroup.

12. (Currently amended) The circuit package as recited in claim 11 wherein said input and output resistances of said driver circuit each have a magnitude in a range of 5 to 12 ohms, inclusive, with said first and second resistances having a magnitude in a range of 35 to 50 ohms, inclusive.

13. (Currently amended) The circuit package as recited in claim 12 wherein said substrate comprises a printed circuit board.

14. (Currently amended) The circuit package as recited in claim 13 wherein said driving circuit is selected from a set of driving circuits consisting of, a buffer, an inverter and an amplifier.

15. (Currently amended) A method of establishing an impedance of a circuit package, said method comprising:

attaching a circuit driver to a dielectric substrate having a first surface and a ~~second surface~~ conductive layer, ~~disposed opposite to said first surface~~ and a via extending therebetween, with a first conductor disposed on said first surface and ~~extending from said via and a second conductor disposed on said second surface and extending from said via~~, with said via placing said first conductor and ~~second conductors~~ said conductive layer in electrical communication, with said driver circuit including an input and an output, with said output being in electrical communication with said first conductor and having an output impedance associated therewith that includes an output resistive component and an output reactance component; and

filling said via with a resistive fill to define a resistance connected between said first conductor and ~~second conductors~~ said conductive layer, with said resistance being

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of sufficient magnitude to define a dominant component of said output impedance.

16. (Currently amended) The method as recited in claim 15 further including connecting said input to an additional conductor disposed on said first surface of said substrate that is connected to an additional via, with said additional via extending from said additional conductor to ~~said second conductor~~ a second conductive layer and filling said additional via with said resistive fill to define an additional resistance connected between said additional conductor and said second conductors conductive layer with input resistive component including said additional resistance and being a dominant component of said input impedance.

17. (Currently amended) The method as recited in claim 15 further including adjusting said output resistance by connecting additional via between said first surface and ~~second conductors~~ said conductive layer and filling said additional via with said resistive fill to create a plurality of resistive vias connected in parallel between said first conductor and ~~second conductors~~ said conductive layer, with said first resistance being inversely proportional to a number of said plurality of said resistive vias.

18. (Currently amended) The method as recited in claim ~~17~~ 16 further including adjusting said input resistance by connecting an additional via between said additional ~~and second conductors~~ conductor and said second conductive layer and filling said additional via with said resistive fill to create a plurality of resistive vias connected in parallel between said additional ~~and second conductors~~ conductor and said second conductive layer, with said additional resistance being inversely proportional to a number of said plurality of said resistive vias.

19. (Original) The method as recited in claim 15 wherein attaching said circuit driver further includes connecting said output to said first conductor at a region positioned spaced-apart from said via, with a length of said first conductor extending between said via and said region defining an interval having a resistance associated therewith, defining an interval resistance, with said output resistive component further including an output resistance of said driver circuit and

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said interval resistance, with said resistance having a magnitude at least twice a magnitude of said output resistance and said interval resistance, combined.

20. (Original) The method as recited in claim 16 wherein attaching said circuit further includes connecting said input to said additional conductor at a region positioned spaced-apart from said additional via, with a length of said additional conductor extending between said additional via and said region defining an interval having a resistance associated therewith, defining an interval resistance, with said input resistive component further including an input resistance of said driver circuit and said interval resistance, with said additional resistance having a magnitude at least twice a magnitude of said input resistance and said interval resistance, combined.

21. (Currently amended) The circuit package as recited in claim 5 wherein said output communicates with said first conductor ~~by way of~~ said first conductor including a conductive bump.

22. (Previously presented) The package as recited in claim 21 wherein said conductive bump is disposed above said via.

23. (Currently amended) The package as recited in claim 22 wherein said conductive bump contacts ~~the first conductor~~ a conductive trace electrically coupled to said via.

24. (Currently amended) A package comprising:
a dielectric substrate having a first surface and a ~~second surface~~ conductive layer,
~~disposed opposite to said first surface~~, and a via extending therebetween, with a
first conductor disposed on said first surface, ~~and a second conductor disposed on~~
~~said second surface~~, with said via placing said first conductor and second
~~conductors~~ said conductive layer in electrical communication;
a circuit mounted to said substrate and including an input and an output, with said output
being in electrical communication with said first conductor and having an output
resistive component associated therewith, with said via having a resistive fill
disposed therein, defining a via resistance connected between said first conductor

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and ~~second conductors~~ said conductive layer, said output having an output impedance being defined at least in part by said output resistive component and said via resistance; and
wherein said ~~output communicates with said first conductor by way of~~ first conductor includes a conductive bump.

25. (Previously presented) The package as recited in claim 24 wherein said conductive bump is disposed above said via.

26. (Currently amended) The package as recited in claim 25 wherein said conductive bump ~~contacts the first conductor~~ is coupled to a conductive trace.

27. (Currently amended) The package as recited in claim 24 26 wherein said substrate includes a plurality of said via, individual ones of a subgroup of which extends of said plurality of via are coupled to the conductive trace and extend between said first surface and ~~second conductors~~ said conductive layer in parallel and have said resistive fill disposed therein to define said via resistance, with said via resistance being inversely proportional to a number of said plurality of vias in said subgroup.

28. (Currently amended) A package comprising:
a dielectric substrate having first surface and a first and second, ~~second, and third~~ conductor layers, having a first resistive via electrically coupling a first conductor on the said first conductor layer surface to a ~~second conductor on the second~~ said first conductor layer, and having a second resistive via electrically coupling a ~~third second~~ conductor on the said first conductor layer to a fourth conductor on the third surface to the second conductor layer, said first and second vias having a resistive fill disposed therein and respectively having a first and second via resistance;

a circuit mounted to said dielectric substrate and including an output having an output resistive component, and including an input having an input resistive component, said output being in electrical communication with said first conductor, and said input being in electrical communication with said ~~third~~ second conductor;

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wherein an output impedance associated with said output is substantially defined by said output resistive component and said first via resistance; and
wherein an input impedance associated with said input is substantially defined by said input resistive component and said second via resistance.

29. (Currently amended) The package as recited in claim 28 wherein said output communicates with said first conductor ~~by way of~~, said first conductor including a first conductive bump.

30. (Previously presented) The package as recited in claim 29 wherein said first conductive bump is disposed above said first via.

31. (Currently amended) The package as recited in claim 29 wherein said first conductive bump contacts ~~the first conductor~~ a conductive trace.

32. (Currently amended) The package as recited in claim 28 wherein said substrate includes a plurality of said first via, a subgroup of which extends between said first surface and ~~second conductors~~ said first conductive layer in parallel and have said resistive fill disposed therein to define said first via resistance, with said first via resistance being inversely proportional to a number of said plurality of vias in said subgroup.

33. (Currently amended) The package as recited in claim 28 wherein said input communicates with said ~~third second~~ second conductor by way of, said second conductor including a second conductive bump.

34. (Previously presented) The package as recited in claim 33 wherein said second conductive bump is disposed above said via.

35. (Cancelled)

36. (Currently amended) The package as recited in claim 28 wherein:

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said output communicates with said first conductor ~~by way of~~ said first conductor
including a first conductive bump disposed above said first via; and
said input communicates with said ~~third~~ second conductor ~~by way of~~ said second
conductor including a second conductive bump disposed above said second via.